

APR 28 2003

Docket No.
END920010026US1

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Application Of: Bernier et al.

Serial No.	Filing Date	Examiner	Group Art Unit
09/885,853	6/20/2001	William D. Coleman	2823

Invention: EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL TO CHIP CONNECTION

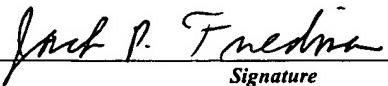
TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

The fee for filing this Appeal Brief is: \$320.00

- A check in the amount of the fee is enclosed.
- The Director has already been authorized to charge fees in this application to a Deposit Account.
- The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 09-0457(IBM)

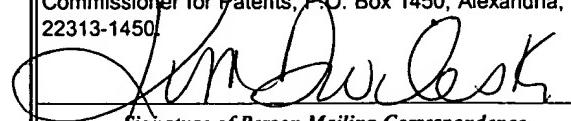
RECEIVED
SEP 15 2003
TECHNICAL CENTER 2800


Signature

Dated: 9/8/2003

Jack P. Friedman
Reg. No. 44,688
Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, NY 12110
(518) 220-1850

I certify that this document and fee is being deposited on 9/8/2003 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Signature of Person Mailing Correspondence

CC:

Kim Dwileski
Typed or Printed Name of Person Mailing Correspondence



#12/Appeal Brief
OK
9/17/03

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Bernier *et al.*

Art Unit: 2823

Serial No.: 09/885,853

Dkt. No.: END920010026US1

Filed: 6/20/01

Examiner: William D. Coleman

Title: **EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL TO CHIP CONNECTION**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF OF APPELLANTS

This Appeal Brief, pursuant to the Notice of Appeal filed July 10, 2003, is an appeal from the rejection of the Examiner dated April 10, 2003.

10

RECEIVED

SEP 15 2003

TECHNOLLOGY CENTER 2800

REAL PARTY IN INTEREST

International Business Machines, Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-6 and 9-18, and 20 are currently pending.

1.000000 1.000000 00000000 00000000 00000000
1.000000 00000000 00000000 00000000 00000000

09/885,853

STATUS OF AMENDMENTS

There are no After-Final Amendments which have not been entered.

SUMMARY OF INVENTION

The present invention discloses an electronic structure, comprising a semiconductor substrate having a first electrically conductive pad thereon, an organic substrate having a second electrically conductive pad thereon, and a solder member electrically coupling the first pad to the second pad. See FIG. 1 and specification, page 3, lines 10-15. A surface area of the first pad exceeds a surface area of the second pad. See specification, page 5, line 21 - page 6, line 2.

The surface area of the first pad may exceed the surface area of the second pad by a factor of at least about 1.2. The surface area of the first pad may exceed the surface area of the second pad by a factor between about 1.1 and about 1.3. the first pad may exceed the surface area of the second pad by a factor of at least about 1.2. The surface area of the first pad may exceed the surface area of the second pad by a factor between about 1.3 and about 2.0.

See specification, page 8, lines 5-9.

The coefficient of thermal expansion (CTE) of the organic substrate mat be between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C. See specification, page 4, lines 3-4.

P may be between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate. See specification, page 11, lines 3-12.

The organic substrate may include an organic material selected from the group consisting

of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof. See specification, page 3, line 19 - page 4, line 2.

The solder member may include a controlled collapse chip connection (C4) solder ball, and the solder member may include a lead-tin alloy. See specification, page 4, lines 5-8.

A distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate may be at least about 0.25 mm. See specification, page 6, lines 2-4. The distance from the centerline of the solder member to the closest lateral edge of the semiconductor substrate may be at least about 0.40 mm. See specification, page 10, lines 14-15.

The electronic structure may further comprise an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal. See FIG. 1 and specification, page 4, lines 13-15.

ISSUES

1. Whether claims 1, 2, 4, 9-13, 15 and 20 are unpatentable under 35 U.S.C. §103(a) over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Kanda et al. (U.S. Patent 6,153,938).
2. Whether claims 3, 5, 6, 14, 16 and 17 are unpatentable under 35 U.S.C. §103(a) over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Kanda et al. (U.S. Patent 6,153,938), and further in view of Chung (U.S. Patent 6,399,178 B1).

3. Whether claim 18 is not unpatentable under 35 U.S.C. §103(a) over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Chung, (U.S. Patent 6,399,178 B1).

Although the Examiner rejected claim 19 under 35 U.S.C. §103(a) over Zhang in view of Chung in the Office Action dated April 10, 2003, said rejection of claim 19 is improper and is not considered in this appeal brief, because claim 19 was canceled in a prior office action response.

GROUPING OF CLAIMS

The claims are grouped as shown in Table 1:

Table 1

Group	Claims	Do Claims of Group Stand or Fall Together?
1	1-6 and 13-17	Yes
2	9-11	Yes
3	12	Yes
4	18	Yes
5	20	Yes

The claims of Group 2 do not stand and fall together with the claims of Group 1, because the claims of Group 2 include the following issue not present in any of the claims of Group 1: whether the condition of a surface area of the first pad exceeding a surface area of the second pad by a factor (of at least about 1.2, between about 1.1 and about 1.3, or between about 1.3 and about 2.0) is obvious over Zhang in view of Kanda.

The claims of Group 3 does not stand and fall together with the claims of Groups 1-2, because the claim of Group 3 includes the following issue not present in any of the claims of Groups 1-2: whether the condition of a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate being at least about 0.25 mm is obvious over Zhang in view of Kanda.

The claim of Group 4 does not stand and fall together with the claims of Groups 1-3, because the claim of Group 4 is being rejected over different references (i.e., over Zang in view of Chung) than are the claims of Groups 1-3.

The claim of Group 4 does not stand and fall together with the claims of Groups 1-4, because the Examiner rejected the claim of Group 4 without providing any argument for the rejection and without providing any references to support the rejection, which did not occur for Groups 1-4.

ARGUMENT

Issue 1

CLAIMS 1, 2, 4, 9-13, 15 AND 20 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER ZHANG ET AL. (U.S. PATENT 6,310,403) B1 IN VIEW OF KANDA ET AL. (U.S. PATENT 6,153,938).

The Examiner rejected claims 1, 2, 4, 9-13, 15 and 20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Kanda et al. (U.S. Patent 6,153,938).

Claim 1

Appellants respectfully contend that claim 1 is not unpatentable over Zhang et al. in view of Kanda, because Zhang in view of Kanda does not teach or suggest each and every feature of claim 1. For example, Zhang in view of Kanda does not teach or suggest “wherein a surface area of the first pad exceeds a surface area of the second pad.”

The Examiner admits that “Zhang fails to teach wherein a surface area of the first pad exceeds a surface area of the second pad.” The Examiner alleges that “Kanda teaches wherein a surface area of the first pad exceeds a surface area of the second pad. See FIG. 1B of Kanda.”

In response to the preceding argument by the Examiner, Appellants note that the Examiner has not identified a first pad and a second pad in FIG. 1B of Kanda, and has not provided any analysis of FIG. 1B of Kanda. Appellants also note that FIG. 1B of Kanda is a cross-sectional view which does not show the spatial extent of surfaces extending normal to said cross-sectional view. Therefore it is impossible to deduce relative surface areas from FIG. 1B of Kanda.

Appellants respectfully reiterate disagreement with the Examiner's allegation that Kanda teaches that a surface area of the first pad exceeds a surface area of the second pad. In "Response to Arguments", the Examiner alleges that FIGS. 1C and 3 of Kanda show the first pad as bump 2 and the second pad as not numbered in FIG. 1C and as shown in FIG. 3. The Examiner seems to be alleging that the pointed nipple 40 in FIG. 3 corresponds to the second pad in claim 1 and is allegedly shown in FIG. 3 as having a smaller surface area than has the bump 2. Thus, the Examiner appear to be identifying the nipple 40 in FIG. 3 as being the alleged pad not numbered in FIG. 1C of Kanda.

In a first response to the Examiner's Reference to FIGS. 1C and 3 of Kanda, Appellants note that FIG. 3 of Kanda is a cross-sectional view which does not show the spatial extent of surfaces extending normal to said cross-sectional view. Therefore it is impossible to deduce the relative surface areas of nipple portion 40 and of bump 2 from FIG. 3 of Kanda.

In a second response to the Examiner's Reference to FIGS. 1C and 3 of Kanda, Appellants contend that the nipple 40 is not a pad distinct from the first pad of bump 2. Rather, the bump 2 and the nipple 40 constitute a single pad. See Kanda, col. 6, lines 6-13 which discloses: "Next, reference numerals 36 and 38 indicate bump forming stages where heating is discontinued while the tool is moved away from the semiconductor IC 1, so as to form a pointed nipple 40. Finally, a reference numeral 50 indicates a bump forming stage where another tool is pressed against the pointed nipple 40 and/or heated, to flatten the pointed nipple 40 so as to form a minor portion of the bump" (emphasis added). Appellants contend that the preceding quote from Kanda demonstrates unequivocally that the nipple 40 is integral with the bump 2 and is a portion of the bump 2. Since the bump 2 and the nipple 40 collectively constitute a single pad

rather than a first pad and a second pad, Appellants maintain that the bump 2 and the nipple 40 cannot be cited as teaching or suggesting “wherein a surface area of the first pad exceeds a surface area of the second pad.”

In application to FIG. 1C of Kanda, the fact that the nipple 40 is not given a reference numeral in FIG. 1C is further evidence that Kanda considers the nipple 40 to be a portion of the bump 2 and not a pad that is distinct from the bump 2. FIG. 1C shows that the semiconductor device 1 is connected to the circuit substrate 6 via a coupling of the nipple portion of the bump 2 to the electrode 7.

Additionally, Appellants respectfully contend that it is not obvious to combine Kanda with Zhang in relation to claim 1.

As a first reason why it is not obvious to combine Kanda with Zhang in relation to claim 1, Appellants respectfully contend that having the surface area of the first pad exceed the surface area of the second pad is incompatible with Zhang who discloses in the very opposite. In FIG. 3, Zhang depicts the surface area of the first pad (between portion 171 and bump 181) is being smaller than the surface area of the second pad 191. Therefore, having the surface area of the first pad exceed the surface area of the second pad would destroy the teaching in FIG. 3 of Zhang.

As a second reason why it is not obvious to combine Kanda with Zhang in relation to claim 1, Appellants respectfully contend that having the surface area of the first pad exceed the surface area of the second pad 191 would offer no utility to Zhang. Zhang’s invention is directed to connecting the substrates 120 and 190 such that the respective interconnects in the substrates 120 and 190 are correctly aligned with each other, and Zhang teaches how to accomplish said

alignment in col. 5, lines 27-36. Appellants maintain that having the surface area of the first pad exceed the surface area of the second pad 191 would not improve said alignment process or provide any other benefit to Zhang, since Zhang teaches a highly successful method of connecting the substrates 120 and 190 with each other.

As a third reason why it is not obvious to combine Kanda with Zhang in relation to claim 1, Appellants respectfully contend that the Examiner has not presented a persuasive reason for modifying Zhang with Kanda. The Examiner alleges: "In view of Kanda, it would have been obvious to one of ordinary skill in the art to incorporate the surface area of the first pad exceeding a surface area of the second pad in the Zhang semiconductor device because the semiconductor chip is flipped over so that the formed bumps are ready to be pressed against a substrate having electrodes (column 6, lines 15-18)." Appellants respectfully contend that the preceding reason given by the Examiner makes no sense, and the Examiner has not provided any analysis to show the relevance of the preceding reason to Zhang. Additionally, the Examiner has not provided any analysis to show the relevance of the preceding reason to the requirement in claim 1 of having the surface area of the first pad exceed the surface area of the second pad, wherein said requirement in claim 1 is what prompted the Examiner to modify Zhang with Kanda.

The Examiner further states: "the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347,

21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the combined teachings discloses a method for coupling a semiconductor substrate.” In response, Appellants maintain that the Examiner has not identified any teaching, suggestion, or motivation in either Zhang or Kanda for modifying Zhang with Kanda. Furthermore, Appellants maintain that Zhang alone teaches how to successfully couple a semiconductor substrate to another substrate, and the Examiner has not identified anything taught or suggested by Kang that meaningfully adds to said teaching by Zhang.

Based on the preceding arguments, Appellants respectfully maintain that the Examiner has not established a *prima facie* case for obviousness in relation to claim 1 and the rejection of claim 1 is therefore improper and should be reversed.

Claims 2, 4, 13, and 15

Since claims 2, 4, 13, and 15 depend from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claims 2, 4, 13, and 15 are not unpatentable under 35 U.S.C. §103(a).

Claim 9

Since claim 9 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 9 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 9 is not unpatentable over Zhang et al. in view of Kanda, because Zhang in view of Kanda does not teach or suggest each and every feature of claim 9. For example, Zhang in view of Kanda does not teach or suggest

“wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2”.

The Examiner admits that “the combined teachings [of Zhang and Kanda] fail to disclose the dimensions of the first and second pad surface area”. The Examiner argues: “However, the combined teachings fail to disclose the dimensions of the first and second pad surface area. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom."

In response to the preceding argument by the Examiner, Appellants point out that the ratio S_1/S_2 , where S_1 and S_2 is the surface area of first pad and second pad, respectively, is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 6, lines 7-13 for a discussion of how S_1/S_2 affects said fatigue life. See Specification, page 6, line 14 - page 8, line 9 for a discussion of test data demonstrating the effect on fatigue life of varying S_1/S_2 . Accordingly, Appellants maintain that claimed ranges of S_1/S_2 is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 9 is not unpatentable over Zhang in view of Kanda. Accordingly, Appellants contend that rejection of claim 9 should therefore be reversed.

Claim 10

Since claim 10 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 10 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 10 is not unpatentable over Zhang et al. in view of Kanda, because Zhang in view of Kanda does not teach or suggest each and every feature of claim 10. For example, Zhang in view of Kanda does not teach or suggest “wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.1 and about 1.3”.

The Examiner admits that “the combined teachings [of Zhang and Kanda] fail to disclose the dimensions of the first and second pad surface area”. The Examiner argues: “However, the combined teachings fail to disclose the dimensions of the first and second pad surface area. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom."

In response to the preceding argument by the Examiner, Appellants point out that the ratio S_1/S_2 , where S_1 and S_2 is the surface area of first pad and second pad, respectively, is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 6, lines 7-13 for a discussion of how S_1/S_2 affects said fatigue life. See Specification, page 6, line 14 - page 8, line 9 for a discussion

of test data demonstrating the effect on fatigue life of varying S₁/S₂. Accordingly, Appellants maintain that claimed ranges of S₁/S₂ is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 10 is not unpatentable over Zhang in view of Kanda. Accordingly, Appellants contend that rejection of claim 10 should therefore be reversed.

Claim 11

Since claim 11 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 11 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 11 is not unpatentable over Zhang et al. in view of Kanda, because Zhang in view of Kanda does not teach or suggest each and every feature of claim 10. For example, Zhang in view of Kanda does not teach or suggest “wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.3 and about 2.0”.

The Examiner admits that “the combined teachings [of Zhang and Kanda] fail to disclose the dimensions of the first and second pad surface area”. The Examiner argues: “However, the combined teachings fail to disclose the dimensions of the first and second pad surface area. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine

experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom.”

In response to the preceding argument by the Examiner, Appellants point out that the ratio S_1/S_2 , where S_1 and S_2 is the surface area of first pad and second pad, respectively, is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 6, lines 7-13 for a discussion of how S_1/S_2 affects said fatigue life. See Specification, page 6, line 14 - page 8, line 9 for a discussion of test data demonstrating the effect on fatigue life of varying S_1/S_2 . Accordingly, Appellants maintain that claimed ranges of S_1/S_2 is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 11 is not unpatentable over Zhang in view of Kanda. Accordingly, Appellants contend that rejection of claim 11 should therefore be reversed.

Claim 12

Since claim 12 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 12 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 12 is not unpatentable over Zhang et al. in view of Kanda, because Zhang in view of Kanda does not teach or suggest each and every feature of claim 10. For example, Zhang in view of Kanda does not teach or suggest “wherein a distance from a centerline of the solder member to a closest lateral edge of the

semiconductor substrate is at least about 0.25 mm”.

Appellants point out that the Examiner has not provided any argument that Zhang in view of Kanda teaches or suggests the preceding feature of claim 12. In fact, the Examiner has not even alleged that Zhang in view of Kanda teaches or suggests the preceding feature of claim 12. Appellants point out that the distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 8, line 10 - page 10, line 19 for a discussion of test data demonstrating the effect on fatigue life of varying the distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate. Accordingly, Appellants maintain that claimed ranges relating to said distance is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 12 is not unpatentable over Zhang in view of Kanda. Accordingly, Appellants contend that the rejection of claim 12 should therefore be reversed.

Claim 20

Since claim 20 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 20 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that the Examiner has not presented any argument in support of the rejection of claim 20. Thus, Appellants contend that the Examiner

has not made a *prima facie* case for obviousness in relation to claim 20 and the rejection of claim 20 should therefore be reversed.

Issue 2

CLAIMS 3, 5, 6, 14, 16 AND 17 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER ZHANG ET AL. (U.S. PATENT 6,310,403) B1 IN VIEW OF KANDA ET AL. (U.S. PATENT 6,153,938), AND FURTHER IN VIEW OF CHUNG (U.S. PATENT 6,399,178 B1).

The Examiner rejected claims 3, 5, 6, 14, 16 and 17 under 35 U.S.C. §103(a) in view of Kanda et al. (U.S. Patent 6,153,938), and further in view of Chung (U.S. Patent 6,399,178 B1).

Since claims 3, 5, and 6 depend from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claims 2, 4, and 6 are not unpatentable under 35 U.S.C. §103(a).

Since claims 14, 16, and 17 depend from claim 12, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claims 14, 16, and 17 are not unpatentable under 35 U.S.C. §103(a).

Issue 3

CLAIM 18 IS NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER ZHANG ET AL. (U.S. PATENT 6,310,403 B1) IN VIEW OF CHUNG (U.S. PATENT 6,399,178 B1).

The Examiner rejected claim 18 under 35 U.S.C. §103(a) as allegedly being unpatentable over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Chung (U.S. Patent 6,399,178 B1).

Appellants respectfully contend that claim 18 is not unpatentable over Zhang in view of Chung, because Zhang in view of Chung does not teach or suggest each and every feature of claim 18. For example, Zhang in view of Chung does not teach or suggest “wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm”. The Examiner has presented no argument supporting that Zhang in view of Chung teaches or suggests the preceding feature of claim 18. In fact, the Examiner admits that “Zhang fails to disclose the dimensions” Thus, Appellants contend that the Examiner has not made a *prima facie* case for obviousness in relation to claim 18 and the rejection of claim 18 is therefore improper.

Additionally, Zhang in view of Chung does not teach or suggest “wherein the underfill material has an elastic modulus of at least about 1 gigapascal”. The Examiner admits that “Zhang fails to disclose ... wherein the underfill material has an elastic modulus of at least about 1 gigapascal.” The Examiner alleges that Chung discloses an underfill material with an elastic modulus of at least about 1 gigapascal. Although Chung discloses the elastic modulus of the underfill material in units of psi (i.e., 2,000,000 psi, column 18, line 61) it is equivalent to Appellants units. In view of Chung, it would have been obvious to one of ordinary skill in the art to incorporate the elastic modulus of Chung into the Zhang semiconductor device because the

rigid adhesive underfill perform is aligned with the substrate (column 14, lines 48-53)."

Appellants note that column 14, lines 48-53 of Chung states: "Rigid adhesive underfill preform 110 is aligned with substrate 30 so that the pattern of solder columns 134 of preform 110 corresponds with the pattern of contact pads 132 of substrate 30." Thus, column 14, lines 48-53 of Chung merely describes how rigid adhesive underfill preform 110 is aligned with substrate 30, but does not provide a reason for the modulus of at least about 1 gigapascal as required by claim 18. Moreover, the preceding statement in Chung does not provide any motivation for a modulus of at least about 1 gigapascal in the underfill 310 in Zhang, and the Examiner has provided no analysis to support why a person of ordinary skill in the art would use an underfill having modulus of at least about 1 gigapascal in the underfill 310 in Zhang. In col. 6, lines 6-10, Zhang states: "after the assembly process, an underfill material 310 is dispensed or injected between substrates 110 and 190 to package or encapsulate the interconnect bumps and the first and second pluralities of interconnects. Material 310 protects the bumps from becoming over stressed during subsequent temperature cycles." Appellants contend that there is no reason, based on the preceding statement in Zhang, why a person of ordinary skill in the art would use an underfill having modulus of at least about 1 gigapascal in the underfill 310 in Zhang. Thus, the combination of Zhang and Chung is not obvious.

Based on the preceding arguments, Appellants respectfully maintain that claim 18 is not unpatentable over Zhang in view of Chung, and that the rejection of claim 18 should be reversed.

SUMMARY

In summary, Appellants respectfully request reversal of the April 10, 2003 rejection of claims 1-6 and 9-18, and 20 under 35 U.S.C. §103(a).

Respectfully submitted,

Jack P. Friedman
Jack P. Friedman
Attorney For Appellant
Registration No. 44,688

Dated: 09/08/2003

Schmeiser, Olsen & Watts
3 Lear Jet Lane - Suite 201
Latham, New York 12110
(518) 220-1850

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Bernier *et al.*

Serial No.: 09/885,853

Filed: 6/20/01

Art Unit: 2823

Dkt. No.: END920010026US1

Examiner: William D. Coleman

**Title: EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL TO CHIP
CONNECTION**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

APPENDIX - CLAIMS ON APPEAL

1. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;
an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and
a solder member electrically coupling the first pad to the second pad.

2. The electronic structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C.

3. The electronic structure of claim 1, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

4. The electronic structure of claim 1, wherein the organic substrate includes an organic material

selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

5. The electronic structure of claim 1, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

6. The electronic structure of claim 1, wherein the solder member includes a lead-tin alloy.

9. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2; and

a solder member electrically coupling the first pad to the second pad.

10. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.1 and about 1.3; and

a solder member electrically coupling the first pad to the second pad.

11. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.3 and about 2.0; and

a solder member electrically coupling the first pad to the second pad.

12. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm.

13. The electronic structure of claim 12, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C.

14. The electronic structure of claim 12, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

15. The electronic structure of claim 12, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

16. The electronic structure of claim 12, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

17. The electronic structure of claim 12, wherein the solder member includes a lead-tin alloy.

18. An electronic structure, comprising:

a semiconductor chip having a first electrically conductive pad thereon;
an organic chip carrier having a second electrically conductive pad thereon;
a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm; and

an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

20. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;
an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.40 mm.